

Applicants submit that the Kumamaru reference does not teach or suggest a second embedded diffusion layer which has an impurity concentration which is at least as high as an impurity concentration of an associated epitaxial layer. Indeed, it is less.

Moreover, Applicants submit that the Aomura reference does not teach or suggest a second embedded diffusion layer which has a depth which is greater than a depth of the associated first embedded diffusion layer.

Applicants respectfully submit that the above-described differences are significant wherein there is simply no suggestion of a structure which addresses the relationship between a depth and impurity concentration of the respective diffusion layers simultaneously. To be sure, since operating speeds and voltages are changed by changing the impurity concentrations and the depths of the first and second diffusion layers of the present invention, it is possible to form the first and second vertical type bipolar transistors on the same substrate wherein the first transistor is a high speed NPN bipolar transistor and the second transistor a high voltage NPN bipolar transistor, and the second embedded diffusion layer of the second transistor is a terminal of such transistor.

In light of the above, Applicants respectfully submit that none of the references cited by the Examiner, either alone or in combination with each other, teach or suggest the semiconductor device of the present invention as now claimed. Accordingly, Applicants respectfully request that all claims presently pending in this case be deemed allowable at this time.

It is further submitted that no fees are due in connection with this application, the office is authorized to deduct said fees from Deposit Account No. 08-2290. If such a withdrawal is made, please indicate the Attorney Docket No. (P97,2608-01) on the account statement.

Respectfully submitted,



(Reg. No. 39,056)

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents Washington, D.C. 20231 on June 19, 2000.

